from the external test pins **210** are latched in the input synchronizing latch **251** immediately after decoding and converted into test signals having respective longer pulse widths, allowing a stable SDRAM stand-alone test to be conducted. Thereafter, the test ACT signal **221**, the test PRC signal **222**, the test Write signal **223**, the test Read signal **224**, the test REF signal **225**, the test address signal **226**, and the test data input signal **227** are supplied to the input synchronizing latch **242** inside the SDRAM core **104** by way of the two-to-one selector **241**.

As described above, in such a configuration, even if the pulse widths of test signals supplied to the external test pins **210** from equipment, such as a tester, are narrower than the period t(CLK) of the internal clock signal **107**, the test signals input from the external test pins **210** are latched into the input synchronizing latch **251** immediately after decoding and converted into test signals having respective longer pulse widths, allowing a stable SDRAM stand-alone test to be conducted. Since there is no effect on signal paths in normal operation, high-speed operation of an interface with the SDRAM core **104** is not lost.

Since an input test signal from an external test pin is synchronized with the internal clock signal **107** when the signal is decoded, the operation of the SDRAM core **104** is delayed by one period t(CLK) of the internal clock signal **107**. By writing a test program for the test equipment that generates a test signal by one period, t(CLK), of the internal clock signal **107** earlier, however, a test can be conducted without causing any problems.

As described above, the semiconductor integrated circuit device and the test method provided by the sixth embodiment makes it possible to conduct a stable SDRAM stand-alone test.

While the present invention has been described with reference to first to sixth illustrative embodiments, the description is not intended to be construed in a limiting sense. It is to be understood that the subject matter encompassed by the present invention is not limited to the embodiments. For example, in the second to sixth embodiments, described above, the external test pins **210** are separate from the external pins **101** which are dedicated solely for testing purposes. However, the external test pins **210** can be connected to the logic circuit **102** and used in normal operation if there is no need to use the external test pins **210** for testing. In addition, other external pins not shown in the figure may also be used as external test pins.

In the first to sixth embodiments, decoders are provided with the SDRAM controller. However, a command decoder can be provided in the SDRAM core **104** for decoding a signal into a command that provides no hindrance to the operation of the SDRAM core **104**, even if the signal is delayed by the decoding. Such a command decoder will still result in the same effects exhibited by the described embodiments.

In addition, in the second to sixth embodiments, the normal/test switch signal **126** is output from the logic circuit as described above. As indicated in the description of the conventional technology, however, it is not necessary to output the normal/test switch signal **126** from the logic circuit. That is, the normal/test switch signal **126** can also be obtained directly from one of the external test pins.

In the embodiments described above, a SDRAM is taken as an example for the present invention. However, the present invention can be applied to other type of RAMs that incorporate command decode systems.

Obviously many modifications and variations of the present invention are possible in the light of the above teachings. It is therefore to be understood that within the scope of the appended claims the invention may by practiced otherwise than as specifically described.

What is claimed is:

1. A semiconductor integrated circuit device comprising:

a logic circuit and a synchronous dynamic random access memory including a core unit, said logic circuit and said synchronous dynamic random access memory being integrated into a single semiconductor chip; and

a synchronous dynamic random access memory control circuit receiving external control signals for said synchronous dynamic random access memory from said logic circuit, and outputting signals to said core unit of said synchronous dynamic random access memory wherein the output signals from said synchronous dynamic random access memory control circuit are internal control signals for controlling said core unit of said synchronous dynamic random access memory.

2. The semiconductor integrated circuit device according to claim **1** further comprising:

external input terminal means for transmitting a first group of internal control signals for said synchronous dynamic random access memory; and

select means for supplying internal control signals to said core unit of said synchronous dynamic random access memory, said internal control signals being obtained by selecting either the first group of internal control signals received from said external input terminal means or a second group of internal control signals received from said synchronous dynamic random access memory control circuit wherein said select means has a first mode selecting the first group of signals received from said external input terminals for testing said semiconductor integrated circuit device with the first group of signals, and a second mode selecting the second group of signals received from said synchronous dynamic random access memory control circuit.

3. The semiconductor integrated circuit device according to claim **1** further comprising:

external input terminal means for transmitting internal control signals for said synchronous dynamic random access memory;

synchronizing means for receiving the internal control signals from said external input terminal means and outputting a first group of internal control signals synchronized with a clock signal of said semiconductor integrated circuit; and

select means for supplying internal control signals to said core unit of said synchronous dynamic random access memory; said internal control signals being obtained by selecting either the first group of internal control signals received from said synchronizing means or a second group of internal control signals received from said synchronous dynamic random access memory control circuit wherein said select means has a first mode selecting the first group of signals received from said synchronizing means, and a second mode selecting the second group of signals received from said synchronous dynamic random access memory control circuit.

4. The semiconductor integrated circuit device according to claim **1** further comprising:

external input terminal means for transmitting external control signals for said synchronous dynamic random access memory:

a command decoder for decoding the external control signals received from said external input terminal

means into a first group of internal control signals for controlling said core unit of said synchronous dynamic random access memory; and

select means for supplying internal control signals to said core unit of said synchronous dynamic random access memory, the internal control signals being obtained by selecting either the first group of internal control signals received from said command decoder or a second group of internal control signals received from said synchronous dynamic random access memory control circuit, wherein said select means has a first mode selecting the first group of signals received from said command decoder, and a second mode for selecting the second group of signals received from said synchronous dynamic random access memory control circuit.

5. A semiconductor integrated circuit device according to claim **1** further comprising:

external input terminal means for transmitting external control signals for said synchronous dynamic random access memory;

synchronizing means for receiving the external control signals from said external input terminal means and outputting external control signals synchronized with a clock signal of said semiconductor integrated circuit; and

a command decoder for decoding the external control signals received from said synchronizing means into a first group of internal control signals for controlling said core unit of said synchronous dynamic random access memory; and

select means for supplying internal control signals to said core unit of said synchronous dynamic random access memory, the internal control signals being obtained by selecting either the first group of internal control signals received from said command decoder or a second group of internal control signals received from said synchronous dynamic random access memory control circuit, wherein said select means has a first mode selecting the first group of signals received from said command decoder and a second mode selecting the second group of signals received from said synchronous dynamic random access memory control circuit.

6. The semiconductor integrated circuit device according to claim **1** further comprising:

external input terminal means for transmitting external control signals for said synchronous dynamic random access memory;

a command decoder for decoding the external control signals received from said external input terminal means into for controlling said core unit of said synchronous dynamic internal control signals random access memory;

a synchronizing means receiving the internal control signals from said command decoder for outputting a first group of internal control signals synchronized with a clock signal of said semiconductor integrated circuit; and

select means for supplying internal control signals to said core unit of said synchronous dynamic random access memory, the internal control signals being obtained by selecting either the first group of internal control signals received from said synchronizing means or a second group of internal control signals received from said synchronous dynamic random access memory control circuit, wherein said select means has a first mode selecting the first signals received from said synchronizing means and a second mode selecting the second signals received from said synchronous dynamic random access memory control circuit.

7. A method for testing a semiconductor integrated circuit device said test method including the steps of comprising:

a logic circuit and a synchronous dynamic random access memory including a core unit, said logic circuit and said synchronous dynamic random access memory being integrated into a single semiconductor chip; and

providing external test signals through external input terminal means to a selector;

providing internal control signals from a synchronous dynamic random access memory control circuit to a selector; and

selecting said external test signals from said external input terminal means, using said selector, for providing the selected signals to a core unit of said synchronous dynamic random access memory for testing.

8. The method for testing a semiconductor integrated circuit device according to claim **7**, wherein the external test signals are internal control signals for testing said core unit of said synchronous dynamic random access memory.

9. The method for testing a semiconductor integrated circuit device according to claim **7**, wherein the external test signals are external control signals for said core unit of said synchronous dynamic random access memory, and is decoded by a decoder to internal control signals provided to said selector.

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